

AMENDMENTS

In the Claims:

1. (Currently Amended) A semiconductor switching circuit device formed on a substrate, comprising:

a first, a second, a third and a fourth field-effect transistor, each of said transistors having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer of the substrate;

a first, a second, a third and a fourth input terminal pad corresponding to the first, second, third and fourth transistors, respectively, the source electrode or the drain electrode of each of the four transistors being connected to the corresponding input terminal pad thereof;

a first common output terminal pad being electrically in direct contact with the source electrode or the drain electrode of the first transistor and being electrically in direct contact with the source electrode or the drain electrode of the second transistor, the two electrodes of the first and second transistors which are electrically in direct contact with the first common output terminal pad not being connected to any of the input terminal pads;

a second common output terminal pad being electrically in direct contact with the source electrode or the drain electrode of the third transistor and being electrically in direct contact with the source electrode or the drain electrode of the fourth transistor, the two electrodes of the third and fourth transistors which are electrically in direct contact with the second common output terminal pad not being connected to any of the input terminal pads;

a first control terminal pad connected to the gate electrodes of the first and third transistors; and

a second control terminal pad connected to the gate electrodes of the second and fourth transistors.

2. (Original) The semiconductor switching circuit device of claim 1, wherein each of the gate electrodes forms a Schottky contact with the channel layer and each of the source electrodes and the drain electrodes forms an ohmic contact with the channel layer.

3. (Original) The semiconductor switching circuit device of claim 1, wherein the substrate is made of a compound semiconductor and each of the transistors is a metal-semiconductor field-effect transistor.

4. (Original) The semiconductor switching circuit device of claim 1, further comprising a first connection connecting the first control terminal pad and the gate electrode of the third transistor, wherein the four transistors are aligned in a direction forming a row of the first, second, third and fourth transistors in this order, and wherein the connection is disposed along the row of the transistors.

5. (Original) The semiconductor switching circuit device of claim 4, wherein the connection comprises a resistor formed between the first control terminal pad and the gate electrode of the third transistor.

6. (Previously Presented) The semiconductor switching circuit device of claim 5, wherein the substrate is made of a compound semiconductor and the resistor comprises a high dopant concentration region.

7. (Original) The semiconductor switching circuit device of claim 4, further comprising a second connection connecting the second control terminal pad and the gate electrode of the second transistor, wherein the two connections intersect each other.

8. (Original) The semiconductor switching circuit device of claim 4, wherein the first, second, third and fourth input terminal pads are disposed on one side of the device so that each of the pads is placed next to the corresponding transistor and wherein the first and second common output terminal pads and the first and second control terminal pads are disposed on a side of the device opposite the side of the device of the four input terminal pads so that the two control terminal pads are placed at both ends of said opposite side of the device and the two common output terminal pads are placed between the two control terminal pads.

9. (Original) The semiconductor switching circuit device of claim 7, wherein the first, second, third and fourth input terminal pads are disposed on one side of the device so that each of the pads is placed next to the corresponding transistor, wherein the first and second common output terminal pads and the first and second control terminal pads are disposed on a side of the device opposite the side of the device of the four input terminal pads so that the two control terminal pads are placed at both ends of said opposite side of the device and the two common output terminal pads are placed between the two control terminal pads, and wherein the first and second connections are disposed between the row of the four transistors and a row of the control terminal pads and the common output terminal pads.

10. (Previously Presented) The semiconductor switching circuit device of claim 8, wherein a portion of the first transistor and a portion of the second transistor are disposed between the first and second input terminal pads, and wherein a portion of the third transistor and a portion of the fourth transistor are disposed between the third and fourth input terminal pads.

11. (Original) The semiconductor switching circuit device of claim 4, wherein each of the gate electrodes forms a Schottky contact with the channel layer and each of the source electrodes and the drain electrodes forms an ohmic contact with the channel layer.

12. (Original) The semiconductor switching circuit device of claim 4, wherein the substrate is made of a compound semiconductor and each of the transistors is a metal-semiconductor field-effect transistor.

13-24 (Cancelled)

25. (Currently Amended) A semiconductor switching circuit device comprising:

a first switch comprising two field-effect transistors each having a source electrode, a gate electrode, a drain electrode and an input terminal pad, and a common output terminal pad for the two transistors of the first switch, the source electrode or the drain electrode of each of the two transistors of the first switch being electrically in direct contact with the common output terminal pad of the first switch, and the source electrode or the drain electrode of each of the two transistors of the first switch which ~~[[are]]~~ is not electrically in direct contact with the common output terminal pad of the first switch being connected to the input terminal pad thereof;

a second switch comprising two field-effect transistors each having a source electrode, a gate electrode, a drain electrode and an input terminal pad, and a common output terminal pad for the two transistors of the second switch, the source electrode or the drain electrode of each of the two transistors of the second switch being electrically in direct contact with the common output terminal pad of the second switch, and the source electrode or the drain electrode of each of the two transistors of the second switch which ~~[[are]]~~ is not electrically in direct contact with the common output terminal pad of the second switch being connected to the input terminal pad thereof; and

two control terminal pads, one of the two control terminal pads being connected to a gate electrode of one of the two transistors of the first switch and a gate electrode of one of the two transistors of the second switch, and another of said two control terminal pads being connected to

a gate electrode of another of the two transistors of the first switch and a gate electrode of another of the two transistors of the second switch.

26. (Original) The semiconductor switching circuit device of claim 25, wherein each of the first and second switch comprises a single pole double throw switch.

27. (Previously Presented) A semiconductor switching circuit device comprising:
four input terminal pads;
two common output terminal pads;
no more than two control terminal pads; and
two single pole double throw switches, each of the switches receiving two high frequency signals through two of the four input terminals and outputting one of the two high frequency signals to one of the two common output terminals in response to a control signal received from one of the control terminals.

28. (Original) The semiconductor switching circuit device of claim 27, wherein the four input terminal pads receive two pairs of balanced signals, and the two common output terminal pads output one of the two pairs of the balanced signals selected by signals applied to the two control terminal pads.

29. (New) A semiconductor switching circuit device comprising:
a first switch comprising two field-effect transistors each having a source electrode, a gate electrode, a drain electrode and an input terminal pad, and a common output terminal pad for the two transistors of the first switch, the source electrode or the drain electrode of each of the two transistors of the first switch being electrically in contact with the common output terminal pad of the first switch, and the source electrode or the drain electrode of each of the two

transistors of the first switch which is not electrically in contact with the common output terminal pad of the first switch being connected to the input terminal pad thereof;

a second switch comprising two field-effect transistors each having a source electrode, a gate electrode, a drain electrode and an input terminal pad, and a common output terminal pad for the two transistors of the second switch, the source electrode or the drain electrode of each of the two transistors of the second switch being electrically in contact with the common output terminal pad of the second switch, and the source electrode or the drain electrode of each of the two transistors of the second switch which is not electrically in contact with the common output terminal pad of the second switch being connected to the input terminal pad thereof; and

two control terminal pads, one of the two control terminal pads being connected to a gate electrode of one of the two transistors of the first switch and a gate electrode of one of the two transistors of the second switch, and another of said two control terminal pads being connected to a gate electrode of another of the two transistors of the first switch and a gate electrode of another of the two transistors of the second switch,

wherein the four input terminal pads are configured to receive two pairs of balanced analog signals and the two common output terminal pads are configured to output one of the two pairs of balanced analog signals received by the four input terminal pads.